O.P.Code: 20EC0442

**R20** 

H.T.No.

## SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR (AUTONOMOUS)

## B.Tech. IV Year I Semester Regular & Supplementary Examinations December-2024 VLSI DESIGN

(Electronics & Communications Engineering)

|       | (Electronics & Communications Engineering)  |                 |           |            |
|-------|---|-----------------|-----------|------------|
| Time: | 3 Hours Ma  | Iax. Marks: 60  |           |            |
|       | (Answer all Five Units $5 \times 12 = 60$ Marks)  |                 |           |            |
|       | UNIT-I  |                 |           |            |
| 1     | a Illustrate the steps involved in NMOS fabrication process with neat                                     | CO <sub>2</sub> | L2        | <b>6M</b>  |
|       | sketches.   |                 |           |            |
|       | b Discuss about body bias effect in the NMOS transistor.  | COL             | 1.2       | 6M         |
|       | OR  |                 |           |            |
| 2     | a Derive the relationship between $I_{ds}$ & $V_{ds}$ in saturated region.                                | CO <sub>2</sub> | L3        | <b>6M</b>  |
|       | <b>b</b> Give the basic steps for IC fabrication.   | CO <sub>2</sub> | <b>L2</b> | <b>6M</b>  |
|       | UNIT-II   |                 |           |            |
| 3     | a What are lambda-based design rules? Explain.  | CO <sub>3</sub> | L1        | <b>6M</b>  |
|       | <b>b</b> Illustrate design rules for wires and MOS transistors.   | CO3             | L2        | 6M         |
|       | OR  |                 |           |            |
| 4     | <b>a</b> Illustrate stick diagram of AND-OR-INVERTER in CMOS design Style.                                | CO3             | L2        | 6M         |
|       | <b>b</b> Explain about Implant and demarcation line in stick diagrams with neat sketches.                 | CO3             | L2        | 6M         |
|       | UNIT-III  |                 |           |            |
| =     |   | CO4             | T 1       | 6M         |
| 5     | a What is switch logic? Explain with an example.  b Explain about page transistors logic with an example. | CO4             | L1<br>L2  | 6M         |
|       | b Explain about pass transistors logic with an example.  OR   | CO4             | LZ        | 6 <b>M</b> |
| 6     |   | CO4             | T 1       | 6M         |
| 6     | <b>a</b> What design methods are used in physical design cycle? Explain each term with suitable diagrams. | CO4             | L1        | 6M         |
|       | b What is routing? Explain about different routing techniques.  | CO4             | <b>L2</b> | <b>6M</b>  |
|       | UNIT-IV   |                 |           |            |
| 7     | Design an Arithmetic and Logic Unit circuit with four functions using                                     | CO4             | L3        | 12M        |
|       | multiplexers and explain its operation.   |                 |           |            |
|       | OR  |                 |           |            |
| 8     | a Compare different types of memory elements.   | CO4             | <b>L4</b> | 6M         |
|       | <b>b</b> Develop the 4x4 array multiplier.  | CO <sub>4</sub> | L3        | <b>6M</b>  |
|       | UNIT-V  |                 |           |            |
| 9     | a Illustrate the architecture of FPGA with neat sketch.   | CO <sub>5</sub> | <b>L2</b> | <b>6M</b>  |
|       | <b>b</b> Discuss about the merits of FPGA over other PLD architectures.                                   | CO <sub>5</sub> | <b>L2</b> | <b>6M</b>  |
|       | OR  |                 |           |            |
| 10    | a What is testing? Explain any three test principles.   | <b>CO5</b>      | L1        | <b>6M</b>  |
|       | <b>b</b> What is controllability and observability? Give examples to explain it.                          | <b>CO5</b>      | L2        | <b>6M</b>  |
|       | *** END ***   |                 |           |            |